Power Shifting Opportunities on BG/Q Using Memory Throttling

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Overview
- Shift power to resources on the critical path
  - Characterize code phases/regions/physics
  - Leverage IBM Blue Gene/Q’s memory throttling
  - Minimize impact on time-to-solution
- Contributions
  - Demonstrated significant power shifting opportunities
  - First to employ real throttling on a supercomputer
  - Linear regression model to guide per-region throttling

Memory Throttling on BG/Q
- BG/Q node architecture
  - 16 A2 cores @ 1.6 GHz, 16 GB memory @ 1.33 GHz
- Kernel_SetPowerConsumptionParam(X)
  - Add X DDR idle cycles for each memory access
  - Node granularity
- Power measurement infrastructure
  - EMON2 high-resolution monitoring
  - Node-board granularity (32 nodes)

LULESH
- Explicit hydrodynamics mini-application
- Five code regions

Optimal memory speed is a function of problem size, concurrency, and code region / kernel

Predicting the Optimal Memory Throttling
- Linear regression model based on HW counters
  - CPU cycles, instructions
  - LSU load/store misses
  - L2 cache misses, prefetching, loads/stores
- Initial model
  \[ f_{\text{min}} = \sum_{i=1}^{n} \left( w_i \cdot \text{counter}_{i} / \text{CPUCycles} \right) \]
- Revised model
  \[ f_{\text{min}} = \sum_{i=1}^{n} \left( w_i \cdot \text{counter}_{i} / \text{CPUCycles} \right) + w_{\text{comp}} \cdot \text{mem} \]

Conclusions & Future Work
- Significant power shifting opportunities with model-based throttling
  - Memory throttling applied on a per-region or per-kernel basis
  - Model predictions result in low performance degradation
  - Savings of up to 20% dynamic power with 3% performance cost
- Future work
  - Study a broader set of applications
  - Shift power on architectures with other throttling capabilities
  - Evaluate non-linear models based on machine learning

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